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(56) Documents Cited
EP 0614328 A US 5290971 A US 5264061 A

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INT CL^6 H01L 21/768 23/12 23/13 23/522 23/538
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(54) Abstract Title
Three-dimensional electronic circuit with multiple conductor layers and method for manufacturing same

(57) The circuit (10) comprises a three-dimensional substrate (12) including a conductive trace (14) on at least one surface of the substrate (12), a thin layer (20) of dielectric material substantially covering a desired portion of the conductive trace(s) (14)on the substrate (12), the dielectric layer (20) including vias (26,28) at selected locations. A coating (16) of conductive material is applied on the dielectric layer (20) and in the vias (26,28) defining a conductive trace (16) in the material to thereby form a multi-layer, interconnected three-dimensional electronic circuit (10). Additional layers of dielectric, material (22,24) and conductive traces (18) may be similarly applied to create the desired number of circuit layers. Moulded-in structural features, and/or vias (38) may be defined in the appropriate layers to accommodate the attachment and/or interconnection of electronic devices (40) to the circuit (10).

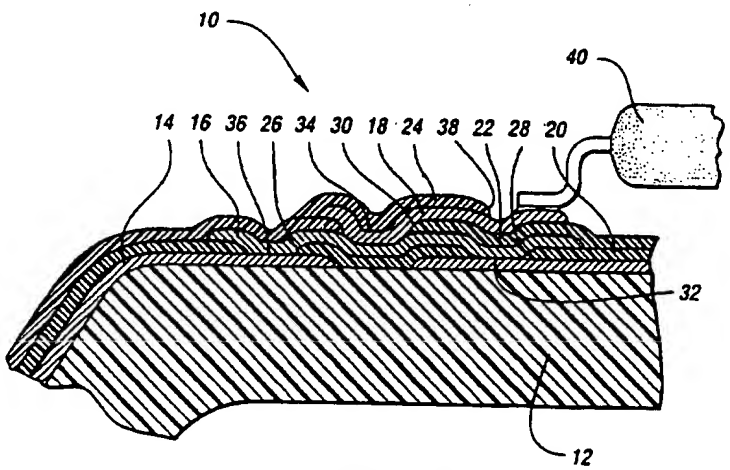

Fig. 2

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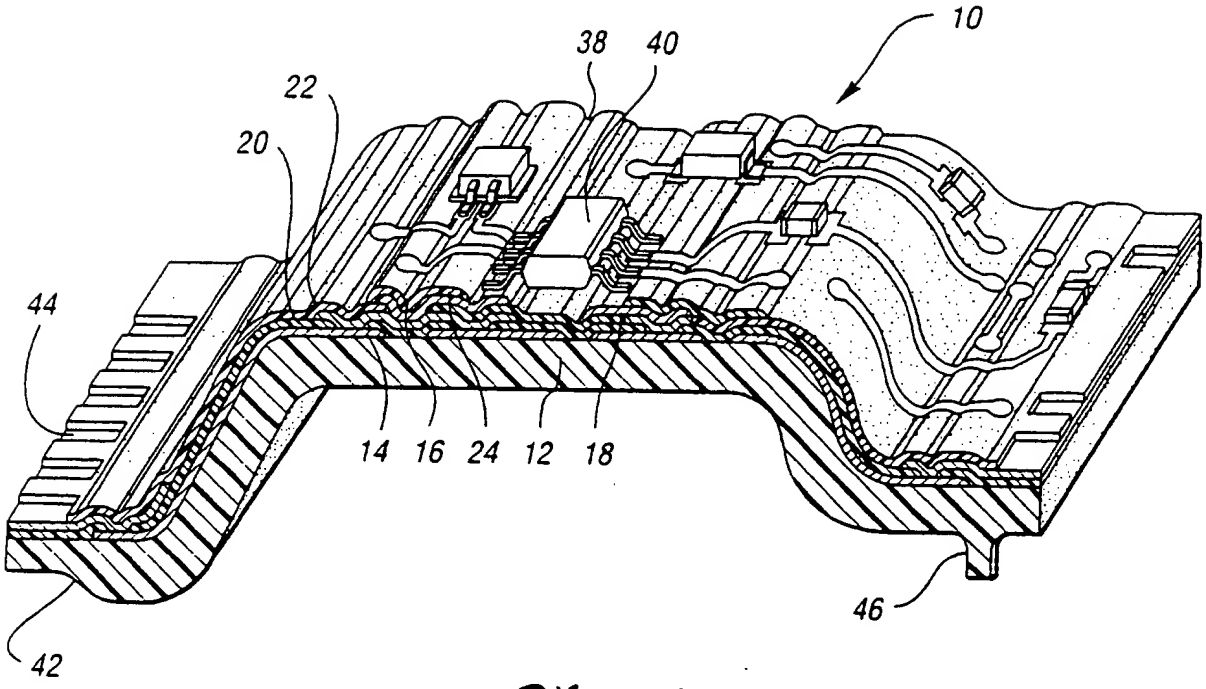

Fig. 1

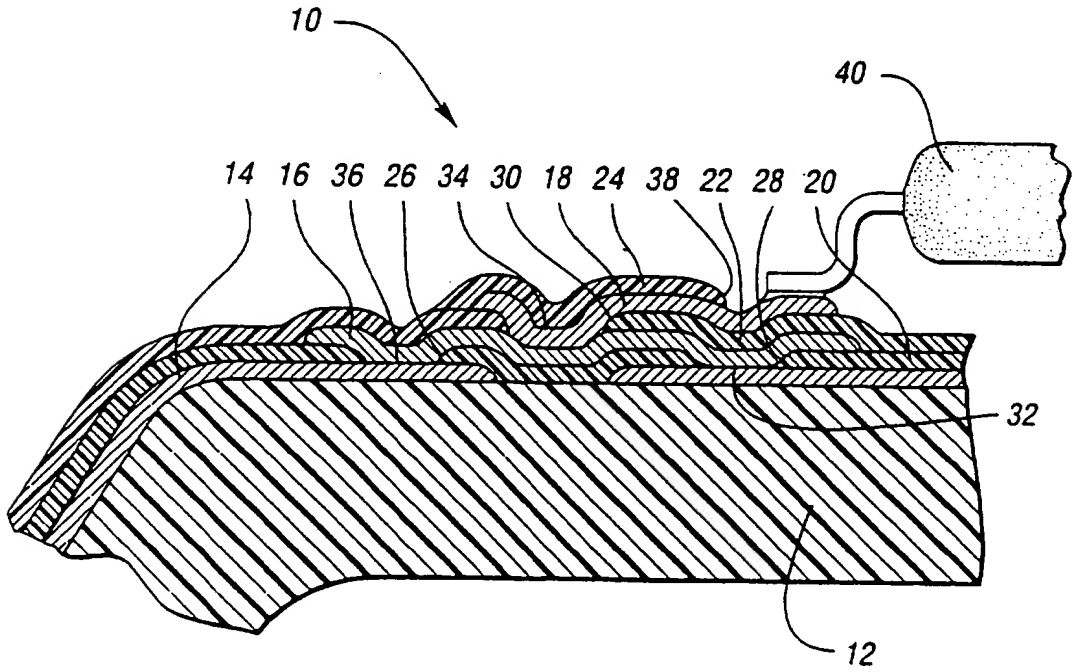

Fig. 2

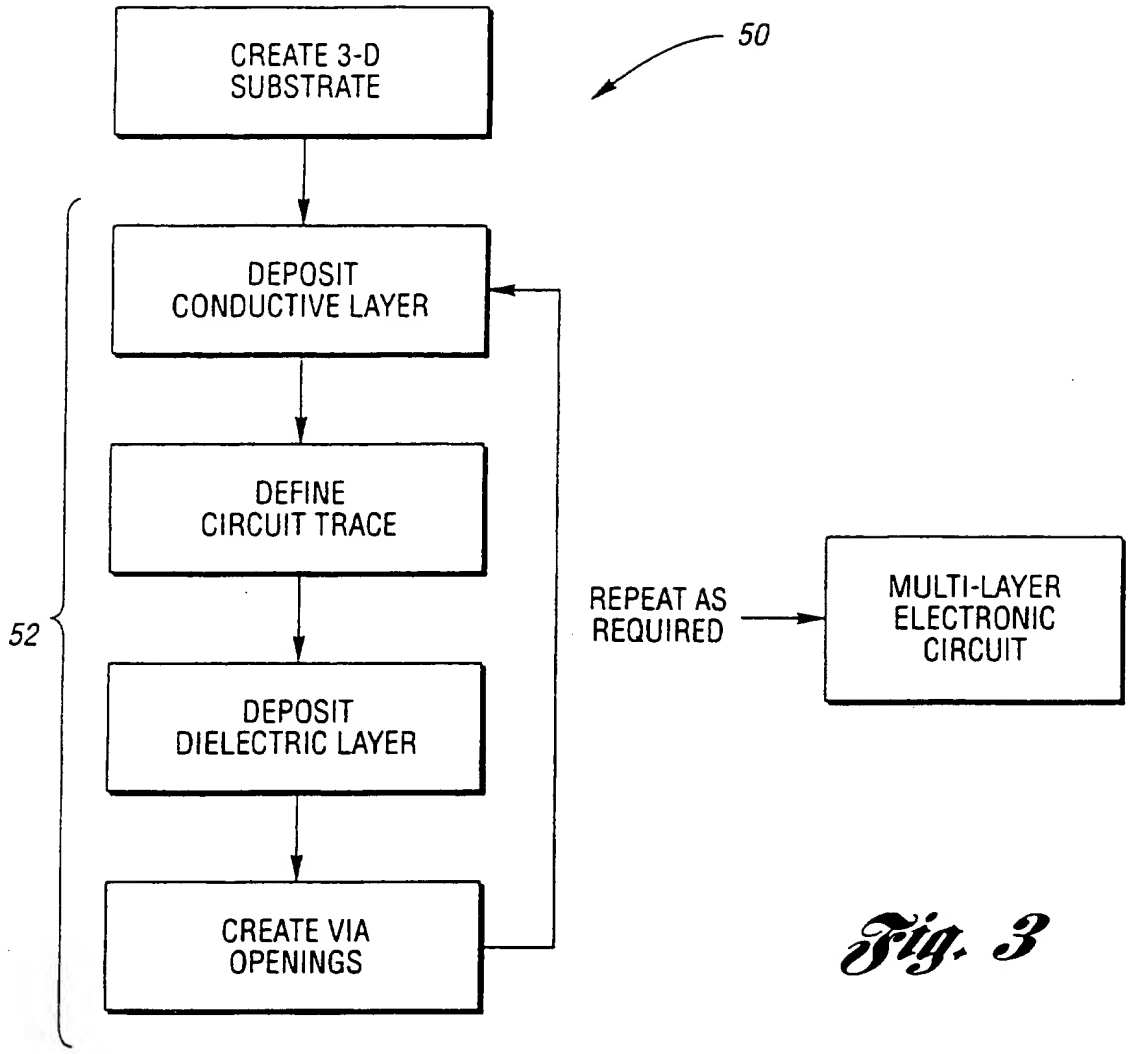
CREATE 3-D SUBSTRATE
50
DEPOSIT CONDUCTIVE LAYER
DEFINE CIRCUIT TRACE
DEPOSIT DIELECTRIC LAYER
CREATE VIA OPENINGS
52
REPEAT AS REQUIRED
MULTI-LAYER ELECTRONIC CIRCUIT

Fig. 3

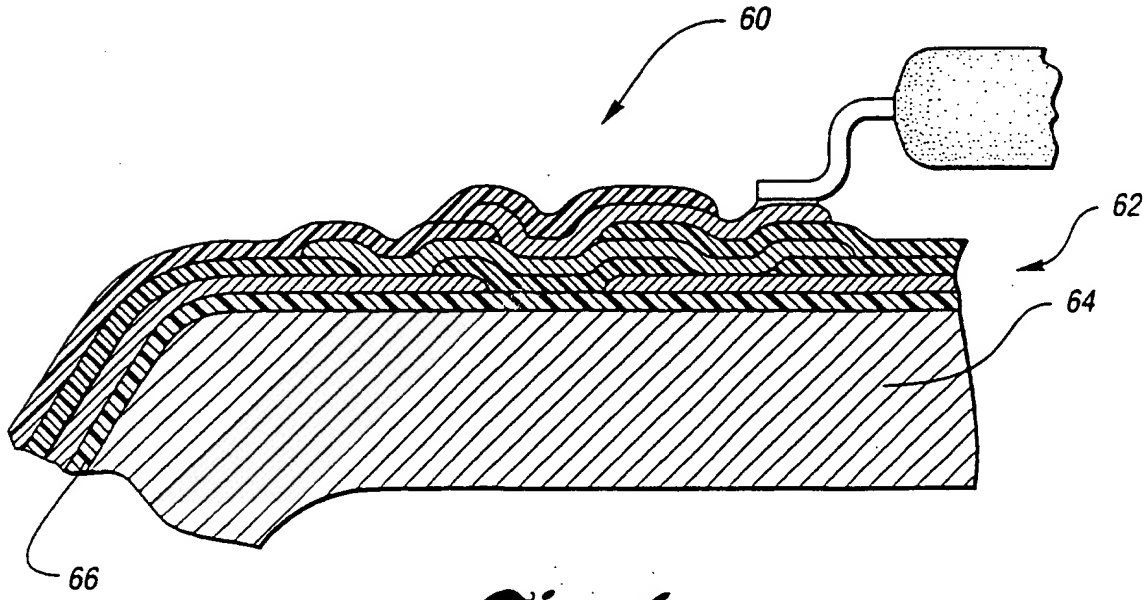
60
62
64
66

Fig. 4

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THREE-DIMENSIONAL ELECTRONIC CIRCUIT WITH MULTIPLE CONDUCTOR LAYERS AND METHOD FOR MANUFACTURING SAME

This invention relates to multi-layer electronic circuits which include a three-dimensional substrate and a plurality of layers of conductive traces fabricated on the substrate and/or intervening layers of dielectric material.

Electronic circuits are commonly manufactured by depositing conductive traces on insulative plastic substrates. Methods of fabricating circuits on three-dimensional (non-planar) substrates including other moulded-in-structural features have also been developed. However, the process for producing the circuitry on three-dimensional surfaces has thus far been limited to one or two layer (i.e., one or both surfaces of the substrate) circuit designs.

According to the present invention, there is provided a method of making a multi-layer three-dimensional circuit which comprises :

providing a three-dimensional substrate;

applying a layer of conductive material in a selected pattern to at least one surface of the substrate; and

fabricating at least one additional circuit layer by :

applying a layer of dielectric material over the conductive trace on the substrate, and

defining vias at selected locations of the dielectric layer for interconnection of the conductive trace on the substrate to other conductive traces: and

applying a layer of conductive material in a selected pattern on the dielectric layer including applying conductive material in the vias to interconnect the conductive trace below the dielectric layer with the conductive trace being applied on the dielectric layer.

The embodiments of the present invention have the advantage of providing a multi-layer three-dimensional circuit including a three-dimensional substrate and a plurality of interconnected layers of conductive traces wherein at least one of the conductive traces is substantially electrically isolated from another of the conductive traces by a thin layer of dielectric material.

The embodiments of the present invention also have the advantage of providing a method of manufacturing a multi-layer three-dimensional circuit by utilising a single three-dimensional substrate upon which a plurality of interconnected circuit traces are applied, defined, and interconnected with thin dielectric coatings therebetween.

The embodiments of the present invention have the further advantage of providing a method of manufacturing a multi-layer three-dimensional circuit in which minimal material is used to create the multiple dielectric and conductive layers which comprise the circuit.

The embodiments of the present invention have the still further advantage of providing a method of manufacturing a multi-layer three-dimensional circuit wherein openings (also referred to herein as vias) may be efficiently created during the circuit fabrication process to provide for connections between conductive traces that are not on the top surface of the circuit *and* additional electronic devices subsequently mounted on the top surface of the circuit.

The method of the embodiments of the present invention includes forming a three-dimensional substrate including an insulative surface, applying an electrical conductor to one or more surfaces of the substrate, defining a circuit trace on the conductive material, then depositing a relatively thin dielectric (non-conductive) layer over the conductive traces. Vias are created in the dielectric layer to create

points of interconnect with subsequently deposited conductive layers, or with other electronic components subsequently mounted on or near the circuit. An additional conductive layer is deposited and defined on the dielectric layer, and the conductive material is deposited in the vias, thereby forming an electrical contact between the first conductive layer and a subsequently applied conductive layer. The process of applying dielectric layers, defining vias, applying conductive layers and defining circuit traces thereon is repeated as many times as necessary to produce the required number of conductive layers for the specific electronic circuit application.

In one embodiment of this method, the electrical conductor material is deposited using electroless plating. The circuit trace is defined on the conductive layer by using known circuit masking and chemical etching techniques. The vias are created in the dielectric layer by laser ablation.

The three-dimensional substrate may be created using a number of typical fabrication methods, including injection moulding, compression moulding, reaction injection moulding, thermal forming, or stamping. The material utilised for the substrate may include polymers, metals, or composites. The substrate may itself be composed of a dielectric material. Alternatively, a relatively conductive material may be utilised for the substrate and, after forming, the substrate may be coated with a thin layer of dielectric material to provide the desired insulative surface prior to defining the first conductive trace on the substrate.

The dielectric layer may be composed of polymers, ceramics or other suitable dielectric material that may be quickly and easily applied as a relatively thin layer on the substrate.

It will be appreciated that various other methods may be utilised for depositing the electrically conductive layer on the substrate and/or dielectric layer surfaces, including electrolytic plating, vapour deposition, sputtering, foil lamination, dispensing conductive polymers or inks and thermal spraying. similarly, other known methods of defining the circuit trace on the conductive layer may be utilised, including laser ablation or machining methods. In addition, the vias may be created in the dielectric layers by other known methods besides laser ablation, such as chemical etching or photoimaging techniques.

Conductive traces may be defined on one or more of the surfaces of the three dimensional substrate prior to coating one or more portions of the circuit traces on the substrate with the desired additional dielectric layers and additional circuit traces.

The three-dimensional multi-layer circuit of the present invention thus includes a three-dimensional substrate upon which a plurality of layers of interconnected conductive traces, with interleaving layers of dielectric material, have been applied to form a complex, three-dimensional electronic circuit.

The three-dimensional substrate may include integrated structural features, such as connectors, sockets, etc., thereby providing a low-cost, three dimensional part with state-of-the-art multi-layer electronic circuitry.

The invention will now be described further, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional perspective view of one embodiment of the present invention;

Figure 2 is an enlarged side view, of a portion of the cross-section of Figure 1;

Figure 3 is a flow diagram of the process of fabricating the three-dimensional circuit according to the present invention; and

Figure 4 is an enlarged side view in cross-section of a portion of an alternative embodiment of the present invention.

Referring now to Figures 1 and 2, the circuit of the present invention, generally designated as 10, includes a three-dimensional (i.e., non-planar) substrate 12 upon which multiple conductive layers 14, 16 and 18, each defining a desired circuit trace are applied and, where desired, interconnected. The multiple layers of circuit traces 14, 16 and 18 are separated by insulative layers 20, 22 and 24 of dielectric material. Openings (or vias) 26, 28 and 30 are created in the dielectric layers (such as vias 26 and 28 in layer 20, and via 30 in layer 22) to allow for interconnection of the conductive circuit traces, such as at 32, 34 and 36. Vias 38 may also be defined in an insulative layer 24 to allow for interconnection of a desired electronic component 40 with one or more of the circuit traces.

Referring now to Figure 3, the method of the present invention includes forming a three-dimensional substrate including an insulative surface, depositing a layer of conductive material on at least one surface of the substrate, defining a circuit trace on the conductive layer, then placing a relatively thin layer of dielectric (non-conductive) material on the conductive trace. Vias are created in the dielectric layer to create sites for interconnection of the circuit trace below the layer with a subsequently applied circuit trace. The operations collectively identified as 52 may be repeated to produce the required number of circuit layers for the specific desired electronic circuit.

The three-dimensional substrate may be created from any material which may be formed to the desired three-dimensional configuration, and which provides the physical characteristics required of the specific part. The dimensions of the substrate will vary with the application and environment in which the finished circuit is to be used. For example, the thickness of the substrate may vary from 0.20 inches to 2.0 inches, with the typical circuit substrates utilised in automotive applications having a thickness of about 0.050 to 0.250 inches. The substrate 12 may be a dielectric material, such as polymers, ceramics, or other conformable composites. Alternatively, the substrate may be created from a conductive material having the desired structural properties. The surface of the conductive substrate is thereafter coated with a dielectric layer, such as substrate 62 of Figure 4.

The conductive layer may be deposited by any of a variety of known methods, including electroless, electrolytic plating, vapour deposition, sputtering, foil lamination, and thermal spraying. The conductive material is preferably copper, but other materials known to be suitable for printed circuit applications, including nickel, may also be utilised. The conductive trace need only be of sufficient thickness to provide a reliable electrically conductive path for the circuit. The thickness of the trace layer typically ranges from about 0.0005 inches to 0.006 inches.

The circuit trace may be defined on the conductive layer by using any of a number of known methods, including masking and chemical etching, laser ablation, or machining methods.

The dielectric layers may be composed of any of a number of known polymers, ceramics, or other dielectric materials that are suitable to insulate the circuit traces.

These layers may be deposited using any of a number of known techniques such as, for example, spray coating, electroplating electrophoritic polymer or dip coating. The dielectric layer is typically substantially thinner, and requires substantially less material, than the substrate. For example, a dielectric layer of from about 0.0005 to 0.003 inches typically provides an adequate insulative layer between two circuit traces.

The substrate may be formed into its three-dimensional configuration by a number of typical fabrication methods which include injection moulding, compression moulding, reaction injection moulding, thermal forming, or stamping.

The vias may be created using known laser ablation, chemical etching, or other material removal techniques.

In one particular embodiment, the three dimensional substrate is injection moulded from 55 percent glass fibre reinforced polyethylene terephthalate (PET). The substrate is then processed through a conventional electroless copper plating line which deposits a flash (i.e., a thin coating, on the order of several micro-inches) of copper over the entire surface of the substrate. The copper coated substrate is then coated with a photosensitive polymer mask, preferably using electrodeposition, then imaged, according to known techniques, to define the circuit patterns. The part is next electrolytically copper-plated to deposit approximately .001 inches of copper. The polymer mask is stripped from the part, and the electroless copper flash removed by chemical etching. The three-dimensional substrate of this embodiment now has a single copper conductive circuit trace on each surface. This part is then dip-coated with an epoxy-acrylate copolymer to form about a .001 inch thick dielectric coating. The polymer coating is then cured using known techniques. Laser ablation is then utilised to create a multitude of approximately .005 inch diameter holes

in the dielectric coating at points of desired interlayer interconnect. The electroless/electrolytic plating process is repeated on the polymer layer, as well as on subsequently applied polymer layers to create the final multi-layer three-dimensional circuit.

As previously described, conductive traces may be defined on one or more of the surfaces of the substrate prior to coating the circuit traces on the substrate, as required, with the desired additional dielectric layers for application of additional circuit traces. The substrate may also include integral structural features, such as connectors, sockets, etc., which features may provide installation sites for electronic components to be mounted on the circuit, or for accommodating installation or interconnection of the completed circuit at its intended site. For example, a recess 42 may be defined in one edge of the substrate so that the finished circuit 10 may be plugged into another board slot or connector for physical installation of the circuit, as well as to interconnect selected layers of the circuit (through vias 44 which provide such interconnection sites) to another board or electrical component. Another example of the moulded-in feature is the locating pin 46, shown in Figure 1. Other examples of three-dimensional structural features and their potential applications are illustrated in Applicant's co-pending application Serial No. U.S. 08/642,722, which is hereby incorporated by reference herein to the extent of that disclosure.

Application Serial No. 08/642,722 is similarly incorporated by reference herein to the extent that it illustrates a method and apparatus for interconnecting circuit traces on opposite surfaces of the three-dimensional substrate, such as might be included in the circuit of the present invention.

It will be appreciated that multiple multi-layer electronic circuits of the present invention might also be physically and/or electronically interconnected as might be suitable for a particular application. Again, application Serial No. 08/642,722 is incorporated by reference herein to the extent that it discloses a method and apparatus for physically interconnecting multiple three-dimensional substrates. Thus, such substrates might each be fabricated to create multi-layer circuits according to the present invention and then physically and/or electrically interconnected as desired.

Referring now to Figure 4, in alternative embodiment 60 of the multi-layer circuit of the present invention is illustrated as including a substrate 62 which comprises a formable conductive material 64 (such as a conductive epoxy or ink) which is formed into its desired three-dimensional configuration, and upon which is then deposited a thin (approximately .001 inches) layer of dielectric material 66 to form the substrate. The subsequent layers of conductive traces and dielectric layers may then be applied as described (and as shown at 52 in Figure 3) to achieve a multi-layer three-dimensional electronic circuit.

CLAIMS

1. A method of making a multi-layer three-dimensional circuit (10) which comprises :

providing a three-dimensional substrate (12);

applying a layer (14) of conductive material in a selected pattern to at least one surface of the substrate (12); and

fabricating at least one additional circuit layer by :

applying a layer (20) of dielectric material over the conductive trace (14) on the substrate (12), and

defining vias (26,28) at selected locations of the dielectric layer (20) for interconnection of the conductive trace (14) on the substrate (12) to other conductive traces (16); and

applying a layer (160 of conductive material in a selected pattern on the dielectric layer (20) including applying conductive material in the vias (26,28) to interconnect the conductive trace (14) below the dielectric layer (20) with the conductive trace (16) being applied on the dielectric layer (20).

2. A method as claimed in claim 1, wherein a dielectric material is provided as the three-dimensional substrate.

3. A method as claimed in claim 1, wherein a thin layer of dielectric material is applied on the surface of the three-dimensional substrate prior to applying the first layer of conductive material.

4. A method as claimed in claim 1, wherein the step of providing a three-dimensional substrate includes defining integral structural features in the substrate.

5. A method as claimed in claim 4, wherein the integral structural features are provided in the substrate

for accommodating installation of the completed circuit at its intended site.

6. A method as claimed in claim 4, wherein the substrate is provided with an integral structural feature which establishes an installation site for an electronic component to be mounted on the circuit.

7. A method as claimed in claim 1, wherein the three-dimensional substrate is fabricated by injection moulding.

8. A method as claimed in claim 1, wherein the layer of conductive material is applied to the substrate by :

applying a flash of copper over the entire surface of the part through electroless plating,

coating the part with a photosensitive polymer mask,

defining an image on the photosensitive polymer mask,

electrolytically plating additional copper over the polymer mask,

stripping the polymer mask from the part, and

removing the electroless copper flash by chemical etching.

9. A method as claimed in claim 1, wherein the layer of conductive material is about 0.001 inches thick.

10. A method as claimed in claim 1, wherein the layer of dielectric material on the at least one additional circuit is about 0.002 inches thick.

11. A method of making a multi-layer three-dimensional printed circuit substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

12. A multi-layer three-dimensional circuit fabricated according a method as claimed in any one of the preceding claims.

The Patent Office

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Application No: GB 9727495.5
Claims searched: all

Examiner: Martyn Dixon
Date of search: 27 March 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K (KHAE, KRD, KRX); H1R (RAS)

Int Cl (Ed.6): H01L (21/768,23/12,23/13,23/522,23/538,27/06); H05K (1/00,3/00,3/46)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0614328 A	(Polyplastics) see e.g. col 3, line 28 to col 5, line 44	1,2,4,7,12
X	US 5290971 A	(Mitsubishi) see e.g. fig 3, col 3, lines 6-12 and col 5, lines 16-23	1,2,4-6, 9,12
X	US 5264061 A	(Motorola) see col 4, lines 12-44	1,2,4,7,12

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.